Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A circuit for detecting an abnormal operation of memory comprising:

a delay circuit for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto; and

a comparison circuit for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other.

Claim 2 (Previously Presented): A circuit for detecting an abnormal operation of memory according to claim 1 wherein an abnormal operation with regard to an access speed of the memory is detected.

Claim 3 (Previously Presented): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for holding address information in case of noncoincidence in response to the noncoincidence signal.

Claim 4 (Previously Presented): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for sounding an alarm when the noncoincidence signal is output.

Claim 5 (Previously Presented): A circuit for detecting an abnormal operation of memory according to claim 1 further comprising a circuit for executing an interruption when the noncoincidence signal is output.

Claim 6 (Original): A circuit for detecting an abnormal operation of memory according to claim 1 wherein a delay time of the output data of the memory can be adjusted in the delay circuit.

Claim 7 (Original): A circuit for detecting an abnormal operation of memory according to claim 1 wherein the memory is a flash memory.

Claim 8 (Previously Presented): An integrated circuit comprising:

a memory which stores data;

a delay circuit which delays an output data from the memory and outputs a delayed data responsive thereto; and

a comparison circuit which compares the output data from the memory and the delayed data, and which outputs a noncoincidence signal when the output data and the

delayed data are not coincident.

Claim 9 (Previously Presented): A method for detecting an abnormal operation of memory comprising:

delaying an output data output from the memory for a predetermined period of time and outputting a delayed data responsive thereto; and

outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other.

Claim 10 (Previously Presented): A method for detecting an abnormal operation of memory according to claim 9 wherein an abnormal operation with regard to an access speed of the memory is detected.

Claim 11 (Previously Presented): A method for detecting an abnormal operation of memory according to claim 9 further comprising holding address information in case of noncoincidence in response to the noncoincidence signal.

Claim 12 (Previously Presented): A method for detecting an abnormal operation of memory according to claim 9 further comprising sounding an alarm when the noncoincidence signal is output.

Claim 13 (Previously Presented): A method for detecting an abnormal operation of memory according to claim 9 further comprising executing an interruption [[on]] of a CPU when the noncoincidence signal is output.

Claim 14 (Currently Amended): A method for detecting an abnormal operation of memory according to claim 9 further comprising rewriting data in the memory when the noncoincidence signal is output.

Claim 15 (Previously Presented): A method for detecting an abnormal operation of memory according to claim 9 wherein a delay time of said delaying is adjustable.

Claim 16 (Original): A method for detecting an abnormal operation of memory according to claim 9 wherein the memory is a flash memory.

Claim 17 (Previously Presented): The integrated circuit according to claim 8, further comprising:

a first latch circuit which stores the output data output from the memory; and

a second latch circuit which stores the delayed data, wherein the comparison circuit receives the output data stored in the first latch circuit and the delayed data stored in the second latch circuit.

Claim 18 (Previously Presented): The integrated circuit according to claim 8, further comprising an address information storing circuit which stores an address information when the comparison circuit outputs the noncoincidence signal.

Claim 19 (New): An integrated circuit comprising:

a memory that stores data;

a delay circuit, directly coupled to the memory, that delays stored data output from the memory for a predetermined period of time and that outputs delayed data responsive thereto; and

a comparison circuit, coupled to the memory and the delay circuit, that compares the stored data output from the memory with the delayed data, and that outputs a noncoincidence signal when the stored data output from the memory and the delayed data are not coincident with each other, the noncoincidence signal indicative of abnormal operation of the memory.

Claim 20 (New): An integrated circuit according to claim 19, wherein abnormal access speed is detected as the abnormal operation of the memory.

Claim 21 (New): An integrated circuit according to claim 19, further comprising a circuit that holds an address of the stored data output from the memory responsive to noncoincidence as indicated by the noncoincidence signal.

Claim 22 (New): An integrated circuit according to claim 19, further comprising a circuit that sounds an alarm responsive to output of the noncoincidence signal.

Claim 23 (New): An integrated circuit according to claim 19, further comprising a circuit that executes an interruption responsive to output of the noncoincidence signal.

Claim 24 (New): An integrated circuit according to claim 19, wherein a delay time of the delay circuit is selectively adjustable.

Claim 25 (New): An integrated circuit according to claim 19, wherein the memory is a flash memory.